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## I<sup>2</sup>C INTERFACE:

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OUTPUT						
RESOLUTION	12 Bits M	INIMUM (11BITS MINIMUM FOR	0-2" AND 0-5mb	RANG	Ξ)	
UPDATE RATE	0.5 ms					
VOLTAGE	SYMBOL	CONDITIONS	MIN	TYP	МАХ	UNITS
HIGH-LEVEL INPUT VOLTAGE	V <sub>IH</sub>	-	0.8 X V <sub>DD</sub>	-	V <sub>DD</sub>	V
LOW-LEVEL INPUT VOLTAGE	V <sub>IL</sub>	-	-	-	0.2 X V <sub>DD</sub>	V
HIGH-LEVEL OUTPUT VOLTAGE	V <sub>OH</sub>	-	V <sub>DD</sub> -0.2	-	V <sub>DD</sub>	V
LOW-LEVEL OUTPUT VOLTAGE	V <sub>OL</sub>	-	0	-	0.2	V
PARAMETER						
OUTPUT SOURCING CURRENT	I <sub>OH_SDA</sub>	SDA @V <sub>OH</sub> , MIN	-1.9	-3.1	-4.8	mA
	I <sub>OH_INT</sub>	INT @V <sub>OH</sub> , MIN	-0.63	-1.2	-1.9	mA
OUTPUT SINK CURRENT	I <sub>OL_SDA</sub>	SDA @V <sub>OL</sub> , MAX	2.3	3.9	6.2	mA
	I <sub>OL_INT</sub>	INT @V <sub>OL</sub> , MAX	0.85	1.7	3.0	mA
LOAD CAPACITANCE AT SDA	C <sub>SDA</sub>	@ 400kHz	-	-	200	рF
PULL-UP RESISTOR	R <sub>I2C_PU</sub>	-	0.5	1	50	kΩ
INPUT CAPACITANCE (EACH PIN)	C <sub>I2C_IN</sub>	-	-	-	10	pF

### TIMING:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	
SCL clock frequency	<b>f</b> <sub>SCL</sub>	100		400	kHz	
Start condition hold time relative to SCL edge	t <sub>HDSTA</sub>	0.1			μs	
Minimum SCL clock low width 1)		0.6			μs	
Minimum SCL clock high width 1)	t <sub>HIGH</sub>	0.6			μs	
Start condition setup time relative to SCL edge	t <sub>susta</sub>	0.1			μs	
Data hold time on SDA relative to SCL edge	t <sub>hddat</sub>	0			μ <b>s</b>	
Data setup time on SDA relative to SCL edge	t <sub>SUDAT</sub>	0.1			μs	
Stop condition setup time on SCL	t <sub>susto</sub>	0.1			μs	
Bus free time between stop condition and start condition	t <sub>BUS</sub>	2			μs	
1) Combined low and biob widths must equal or exceed minimum SCLK period						

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NOTE: THEF

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ON IAGRAM:			
TA tHDDAT			t <sub>B</sub> us
RE ARE THREE ADJUSTMENTS To ding a start-stop condition withou mmunication error for the next c e is applied. An additional start of munication. restart condition—a falling SDA tes the same situation. The next ect communication. lling SDA edge is not allowed be address with the first bit 0. SD	O THE I <sup>2</sup> C IMPLEMENTATION COMPARED W ut any transitions on the CLK line (no clock pu communication, even if the next start condition condition must be sent, which results in restor edge during data transmission when the CLK t communication fails, and an additional start of etween the start condition and the first rising S A must be held low from the start condition the	/ITH THE ORIGINAL I <sup>2</sup> C PROTOCOL: ilses in between) creates is correct and the clock ation of proper Clock line is still high— condition must be sent for CL edge. If using an rough the first bit	
I <sup>2</sup> C COMMUNICATION: S 6 5 4 3 2 1 0 R DEVICE SLAVE ADDRESS [6:0] SLA	A       15       14       13       12       11       10       9       8       A       7       6       5       4         I	3 2 1 0 N S SURE MASTER A [7:0] NACK	<ul> <li>S Start Condition</li> <li>Device Slave Address (example: Bit 5)</li> <li>Data Bit (example: Bit 2)</li> <li>Read/Write Bit (example: Read=1)</li> <li>Acknowledge (ACK)</li> <li>No Acknowledge (NACK)</li> </ul>
IOSTIC FEATURES: P1 J OFFERS A FULL SUITE O RATION. THE DIAGNOSTIC STATUS OF THE 2 MSBs OF T PUT AT 3FFF <sub>H</sub>	F DIAGNOSTIC FEATURES TO ENSURE R STATES ARE INDICATED BY A TRANSMI HE BRIDGE HIGH BYTE DATA OR BY A S	OBUST SYSTEM SSION OF SATURATED	S Stop Condition Status Bit
STATUS BITS Bs OF OUTPUT PACKAGE)	DEFINITION		
00	NORMAL OPERATION, GOOD DATA	PACKET	
01	RESERVED (WILL NOT BE SEEN DURIN	G OPERATION)	
10	STALE DATA: DATA THAT HAS ALREA	DY BEEN FETCHED	

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STATUS BITS (2 MSBs OF OUTPUT PACKAGE)	DEFINITION
00	NORMAL OPERATION, GOOD DATA PACKET
01	RESERVED (WILL NOT BE SEEN DURING OPERATION)
10	STALE DATA: DATA THAT HAS ALREADY BEEN FETCHED SINCE THE LAST MEASUREMENT CYCLE. NOTE: IF A DATA FETCH IS PERFORMED BEFORE OR DURING THE FIRST MEASUREMENT AFTER POWER-ON RESET, THEN "STALE" WILL BE RETURNED, BUT THIS DATA IS ACTUALLY INVALID BECAUSE THE FIRST MEASUREMENT HAS NOT BEEN COMPLETED
11	DIAGNOSTIC CONDITION EXISTS

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B 22863 E P1J-DWG SCALE NONE CAD: SOLIDWORKS SHEET 2 OF 3

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SPI READINGS WILL BE PROVIDED IN A DUPLEX 3-WIRE READ ONLY FORMAT. THE ENTIRE OUTPUT PACKET CONSISTS OF 4 BYTES (32 bits). THE HIGH BYTE OF THE PRESSURE DATA IS TRANSMITTED FIRST, FOLLOWED BY THE LOW BYTE. THEN 14 bits OF OPTIONAL TEMPERATURE DATA [(TC13:0]) ARE SENT. THE LAST 2 bits OF THE FINAL BYTE ARE "DO NOT CARE" AND SHOULD BE IGNORED. IF THE OPTIONAL TEMPERATURE DATA IS REQUIRED, PLEASE CONTACT THE KAVLICO SALES TEAM. FOR ALL OTHER APPLICATIONS, THE READ CAN BE TERMINATED AFTER THE 2ND BYTE.

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### SPI INTERFACE:

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OUTPUT						
RESOLUTION	12 Bits N	NINUMUM (11 BITS MINIMUM FOR	2 0-2" AND 0-5m	b RANC	GE)	
UPDATE RATE	0.5 ms					
VOLTAGE	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-LEVEL INPUT VOLTAGE	V <sub>IH</sub>	-	0.8 X V <sub>DD</sub>	-	V <sub>DD</sub>	V
LOW-LEVEL INPUT VOLTAGE	V <sub>IL</sub>	-	-	-	0.2 X V <sub>DD</sub>	V
HIGH-LEVEL OUTPUT VOLTAGE	V <sub>OH</sub>	-	V <sub>DD</sub> -0.2	-	V <sub>DD</sub>	V
LOW-LEVEL OUTPUT VOLTAGE	V <sub>OL</sub>	-	0	-	0.2	V
PARAMETER						
OUTPUT SOURCING CURRENT	I <sub>OH_MISO</sub>	MISO @V <sub>OH</sub> , MIN	-1.9	-3.1	-4.8	mA
	I <sub>OH_SS</sub>	ss @v <sub>oh</sub> , min	-0.63	-1.2	-1.9	mA
OUTPUT SINK CURRENT	I <sub>OL_MISO</sub>	MISO @V <sub>OL</sub> , MAX	2.3	3.9	6.2	mA
	I <sub>OL_SS</sub>	SS @V <sub>OL</sub> , MAX	0.85	1.7	3.0	mA
INPUT CAPACITANCE (EACH PIN)	C <sub>I2C_IN</sub>	-	-	-	10	pF

### **OUTPUT PACKET WITH POSITIVE EDGE SAMPLING:**



3

PACKET = [ {S(1:0), B(13:8)}, { B(7:0)}] WHERE S(1:0) = STATUS bits OF PACKET (NORMAL, STALE DIAGNOSTIC) B(13:8) = UPPER 6 bits OF 14-bit PRESSURE DATA B(7:0) = LOWER 8 bits OF 14-bit PRESSURE DATA HIZ = HIGH IMPEDANCE

#### TIMING:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency	<b>f</b> <sub>SCL</sub>	50		800	kHz
SS drop to first clock edge	t <sub>HDSS</sub>	2.5			μs
Minimum SCLK clock low width 1)	t <sub>LOW</sub>	0.6			μs
Minimum SCLK clock high width 1)	t <sub>HIGH</sub>	0.6			μs
Clock edge to data transition	t <sub>CLKD</sub>	0		0.5	μs
Rise of SS relative to last clock edge	t <sub>SUSS</sub>	0.1			μs
Bus free time between rise and fall of SS	t <sub>BUS</sub>	2			μs
1) Combined low and high widths must equal or exceed minimum SCLK perio	d				

Combined low and high widths must equal or exceed minimum SCLK period

#### **TIMING DIAGRAM:**



NOTE: THE MISO LINE IS SETUP TO CHANGE STATE ON THE FALLING EDGE OF THE SCLK CLOCK. ACCORDINGLY, THE MASTER SHOULD SAMPLE THE DATA ON THE RISING EDGE OF THE SCLK SIGNAL.

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# **DIAGNOSTIC FEATURES:**

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THE P1J OFFERS A FULL SUITE OF DIAGNOSTIC FEATURES TO ENSURE ROBUST SYSTEM OPERATION. THE DIAGNOSTIC STATES ARE INDICATED BY A TRANSMISSION OF THE STATUS OF THE 2 MSBs OF THE BRIDGE HIGH BYTE DATA OR BY A SATURATED OUTPUT AT 3FFF.,

STATUS BITS (2 MSBs OF OUTPUT PACKAGE)	
00	NORMAL OPER
01	RESERVED (WILI
10	STALE DATA: D SI NOTE: IF A DAT, DURING THE FI RESET, THEN "S IS ACTUALLY II HAS NOT BEEN
11	DIAGNOSTIC C

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**15** SPI COMMUNICATION

DEFINITION

RATION, GOOD DATA PACKET

L NOT BE SEEN DURING OPERATION)

DATA THAT HAS ALREADY BEEN FETCHED INCE THE LAST MEASUREMENT CYCLE. A FETCH IS PERFORMED BEFORE OR IRST MEASUREMENT AFTER POWER-ON STALE" WILL BE RETURNED, BUT THIS DATA **NVALID BECAUSE THE FIRST MEASUREMENT** I COMPLETED

2

CONDITION EXISTS

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B	CODE IDENT NO. 22863		P1J-DWG			E	
SCALE	NONE	CAD: SOLIDWORKS		SHEET	3	OF	3

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